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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/684,871	Applicant(s) MOLL ET AL.	
	Examiner Hong Cho	Art Unit 2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-3, 6-10, 12-15, 17, 18 and 20 is/are rejected.
- 7) ☒ Claim(s) 4, 5, 11, 16 and 19 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) ☒ Notice of References Cited (PTO-892) | 4) ☐ Interview Summary (PTO-413) |
| 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. ____. |
| 3) ☐ Information Disclosure Statement(s) (PTO/SB/08) | 5) ☐ Notice of Informal Patent Application |
| Paper No(s)/Mail Date ____. | 6) ☐ Other: ____. |

DETAILED ACTION

Claim Objections

1. Claim 7 is objected to because of the following informality:

Re claim 7, line 3, "HT" should be spelled out.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102(e) that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 6, 8-10, 12-15, 17, 18 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Kaniz et al (US 7099325), hereinafter referred to as Kaniz.

Re claim 1, Kaniz discloses a multiport switch with a plurality of receiver ports (*a receiver port*, figure 3, elements 301-304), transmitter ports (*a plurality of destination modules*, figure 3, element 311-314), a circuit comprising internal rules checker (IRC) and port vector queue (PVQ) (*a routing circuit coupled to receive a plurality of packets*

from the receiver port, figure 3), receiving a packet at one of receiver ports, splitting a header portion from data portion of the packet, making forwarding decision for the packet based on the header information, outputting its forwarding decision in the form of a forward descriptor (a routing signal) and transmitting the packet to the appropriate output port (programmably configured, for each received packet, to select a destination module for said received packet by calculating a routing signal using one or both of programmably selected control and data information extracted from the received packet as said received packet is being received, column 7, lines 21-22; lines 29-32). Kaniz discloses a circuit comprising IRC with a decision making engine (a first table, figure 3, element 245) that makes frame forwarding decisions (to generate a rule table output) for data packets by using one of header information, where source and destination information are used for filtering packets according to one of internal rules in the IRC (a first table containing a plurality of independent rules that process data from the received packet in parallel as each packet is received to generate a rule table output for each rule contained in the first table, column 6, lines 9-22; lines 46-51), and an address lookup table (a second table) used by IRC in generating forwarding descriptor after filtering result of the packet for determining correct forwarding information for a received frame (a second table containing a plurality of paths that combine the rule table outputs from the first table to generate a routing signal for the received packet, column 6, lines 36-38; column 7, lines 61-64).

Re claims 2 and 17, Kaniz discloses directly outputting the routing signal as a routing result from the routing circuit to switch the received packet to a destination module identified by the routing result (column 7, lines 65 to column 8, line 1).

Re claims 3 and 18, Kaniz discloses using the routing signal as an index (*a frame pointer*) to a routing table (*an external memory*, figure 3, element 170) to output a routing result from the routing circuit to switch the received packet to a destination module identified by the routing result (column 5, lines 55-57; column 6, lines 42-45).

Re claim 6, Kaniz discloses receiving a plurality of packets at a plurality of receiver ports (*a plurality of input virtual channels*, figure 3, elements 301-314) (*a plurality of interleaved packets on a respective plurality of input virtual channels*) and supplying a frame pointer, decoded from a forwarding descriptor, to the output queues (*the routing signal is encoded in the form of an output virtual channel that is used by the multiprocessor switching chip to route packets to destination modules on the multiprocessor switching chip*, column 6, lines 42-45).

Re claim 8, Kaniz discloses generating forwarding descriptor for making forwarding decision for the packet based on the header information (*routing circuit calculates the routing signal without requiring processor intervention*, column 6, lines 10-15).

Re claim 9, Kaniz discloses transmitter ports (*a plurality of destination modules*, figure 3, element 311-314) with management queue (*a packet manager input circuit*, figure 3) and inherent transmit circuit to transmit packets on an integrated circuit.

Re claims 10 and 15, Kaniz implicitly discloses specifying a location of data information in the received packet that is to be extracted by the routing circuit in splitting a header portion from data portion of the packet.

Re claim 12, Kaniz discloses an IRC (*a first table*, figure 3, element 245) with a decision making engine that makes frame forwarding decisions for data packets by using one of header information according to one of internal rules in the IRC (*each rule in a first table selects data from the received packet and compares the selected data to an operand of the rule to generate a true/false result for each comparison which may be output as the rule table outputs*, column 6, lines 9-22; lines 45-51).

Re claim 13, Kaniz discloses an address lookup table used by IRC in generating forwarding descriptor for determining correct forwarding information for a received frame (*a second table evaluates rule table outputs from the first table to generate a routing signal that may be output directly as a first routing result*, column 6, lines 36-38; column 7, lines 61 to column 8, line 1).

Re claim 14, Kaniz discloses transmitting a packet to one of ports in a multiport switch (*routing a packet to one of a plurality of destination in a processor circuit*, column 7, lines 31-32). Kaniz discloses receiving a packet at one of ports (*receiving at least a first packet on a receiver port of the processor circuit*, column 7, lines 31-32), splitting a header portion from data portion (*decoding said first packet to extract packet data and packet control information*, column 7, lines 21-22), making forwarding decision for the packet based on the header information (*calculating a routing decision for the packet data based upon programmably selected information from the packet data or packet*

control information while the first packet is being received, column 6, lines 9-11), outputting its forwarding decision in the form of a forward descriptor (generating a routing result based upon the routing decision, column 6, lines 36-37), and transmitting the packet to the appropriate output port (transferring the first packet to a destination in the processor circuit identified by the routing result, column 7, lines 29-30).

Re claim 20, Kaniz discloses a circuit for transmitting packets received on receiver ports (*input virtual channels*, figure 3, elements 301-304) to the appropriate output ports (*output virtual channels*, figure 3, elements 311-314) (*a hash and route circuit for routing packet data extracted from a packet received on an input virtual channel to an output virtual channel*, column 7, lines 21-22). Kaniz discloses an IRC with a decision making engine (*a rule table*, figure 3, element 245) that makes frame forwarding decisions for data packets by using one of header information, where source and destination information (*at least one byte from the packet data*, figure 4, elements 401 and 402) used for filtering packets according to one of internal rules in the IRC (*a rule table comprising a plurality of programmable rules, where each rule selects at least one byte from the packet data or the input virtual channel information and compares the selected at least one byte to an operand of the rule to generate a true/false result for the rule*, column 6, lines 9-22; lines 46-51), and an address lookup table (*a path table*) used by IRC in generating forwarding descriptor (*path data*) after filtering result of the packet for determining correct forwarding information for a received frame (*a path table comprising a plurality of entries which search for selected true/false results from the rule table and output path data from a matching entry*, column 6, lines 36-38; column 7, lines

61-64), and a routing table (*an external memory*, figure 3, element 170), where using the path data from the path table as an index (*a frame pointer*) to a routing table (column 5, lines 55-57; column 6, lines 42-45).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.
5. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kaniz in view of Keck et al (US 20040122973), hereinafter referred to as Keck.

Re claim 7, Kaniz discloses all of the limitations of the base claim, but fails to disclose a switch hop route signal that is used to route the received packet over an HT switch device coupled to the multiprocessor switching chip. Keck discloses using hyper transport (HT) link to couple processors and peripheral devices (paragraph [0004], lines 1-3). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Kaniz to implement HT link of Keck for the benefit of allowing high speed data transfer resulting in high throughput.

Allowable Subject Matter

6. Claims 4, 5, 11, 16 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement for reasons for allowance.

7. Claims 4 and 5 are allowable over the prior art of record since the cited references taken individually or in combination fail to particularly teach or fairly suggest hashing (extracting in claim 5) predetermined data from the received packet to generate a hash (extract in claim 5) value, wherein the hash (extract in claim 5) value and the routing signal are used to generate an index to a routing table to output a routing result to switch the received packet to a destination module identified by the hash (extract in claim 5) value and the routing result.
8. Claims 11 and 16 are allowable over the prior art of record since the cited references taken individually or in combination fail to particularly teach or fairly suggest specifying a location of an offset pointer in the received packet, where said offset pointer specifies a location of data information in the received packet that is to be extracted by the routing circuit.
9. Claim 19 is allowable over the prior art of record since the cited references taken individually or in combination fail to particularly teach or fairly suggest extracting and hashing a plurality of bytes from the packet data or packet control information to generate a hash value that is used to index into a routing table to output a routing result.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hong Cho whose telephone number is 571-272-3087. The examiner can normally be reached on Mon-Fri during 7 am to 4 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on 571-272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

hc
Hong Cho
Patent Examiner
5/4/07